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Third Military and Aerospace Programmable Logic Devices International Conference (MAPLD'2000)

ELECTRONIC digital systems design in modern aerospace applications is no longer dominated by application specific integrated circuits (ASICs) or small-scale integration/medium-scale integration (SSI/MSI) devices as a result of the growing popularity of programmable logic devices (PLDs). PLDs utilize programmable switches permitting logic blocks and their interconnections to be reprogrammed or reconfigured outside the foundry. This can be done, depending on the physical implementation, either in the engineer's laboratory or in situ in the vehicle or spacecraft. High-reliability-grade field programmable gate arrays (FPGAs) for aerospace applications range in density from tens of thousands up to approximately one million logic gates plus embedded SRAM blocks on a single chip, enabling system-level integration capabilities in a programmable format. The hardware programmability of these chips opens up many new design possibilities, and therefore PLDs are at the center of the attention of a large community of designers, practitioners, researchers, and scientists.

This issue of the *Journal of Spacecraft and Rockets* contains a selection of four papers presented at the 3rd Military and Aerospace Programmable Logic Devices (MAPLD) International Conference, MAPLD'2000. The MAPLD Conference is an annual event, sponsored by NASA; the National Security Agency; Johns Hopkins University, Applied Physics Laboratory; Electronics Radiation Characterization; AIAA; and the Institute of Electrical and Electronics Engineers Aerospace and Electronic Systems Society. It is held each September at the Johns Hopkins University, Applied Physics Laboratory in Laurel, Maryland. Established in 1998, the conference has become a focal point for addressing a wide range of digital engineering problems in space flight systems with a view to their practical solution. Over the years, the MAPLD conference has attracted attention and enthusiastic support from many programmable-logic specialists across the aerospace industry, academia, and PLD manufacturers and has developed into a popular forum for discussion of application aspects of programmable devices and adaptive computing systems in military and aerospace systems.

The papers included in this issue represent three of five technical sessions of MAPLD'2000. The paper entitled "Field-Programmable Gate-Array-Based Graph Coloring Accelerator" by L. M. Pochet, M. L. Linderman, S. L. Drager, and R. L. Kohler was a part of the conference session "Military and Aerospace Applications." The paper describes a hardware accelerator that implements a graph-coloring algorithm based on a solution of the Latin square problem. The device is implemented using XILINX Virtex 1000 FPGAs and a high-level programming tool including the JAVA hardware description language (JHDL). The accelerator is targeted at efficient implementation of routing for wave division multiplexing (WDM) optical communication systems in satellite constellations and multihop radio communications.

The next two papers fall into the thematic domain of the conference session "Devices, Elements, and Technologies." The paper entitled "Advances in Data Handling Systems for Space Experiment Control" by J. C. Lyke, P. A. Brezna, and K. Avery discusses on-board data handling. The paper describes design and development aspects of the data handling system for the electronics testbed in the Space Test Research Vehicle Satellite (STRV-1d). The data handling system acts as a plug-and-play experiment "brokering" system, controlling a set of nine experiments that evaluate the operation of emerging electronics and sensor technologies in the space environment. Future extensions of the concept for experiment data handling are discussed.

The paper "Cellular Automata-Based Reconfigurable Systems as Transitional Approach to Gigascale Electronic Architectures" by J. C. Lyke, G. W. Donohoe, and S. P. Karna discusses a new technology for programmable devices. The paper is concerned with the emerging field of molecular electronics, describing a design approach to gigascale electronic architectures that can be beneficial to future aerospace electronic systems. The authors propose a cellular automata-inspired periodic spatial structure that involves the use of three-dimensional, paper-thin, ultra-high-density, multichip modules to assemble a reconfigurable design that is scalable. Details of gigascale demonstrations of the cellular FPGA concept in silicon are presented.

The paper "New Methodology for Simulation of Soft Errors in Digital Processors" by S. Rezgui, R. Velazco, S. Rodríguez, and R. Ecoffet was presented in the conference session "Radiation Environments and Effects." The paper describes a new strategy for characterization and quantification of the effects of single event upsets (SEUs) on microprocessor-based digital architectures operating under radiation. The approach relies on injection of SEU faults concurrently with the execution of a program and is based on a code emulating an upset (CEU) software tool. A dedicated test system called Testbed for Harsh Environment Studies on Integrated Circuits for SEU ground testing purposes is described. The authors report excellent agreement between predicted and measured error rates.

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